**Lab #2 Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_**

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| --- | --- | --- |
| **Item** | **Grade** | **Points** |
| **Req** | **40** |  |
| **B Func** | **10** |  |
| **A Func** | **10** |  |
| **Github** | **5** |  |
| **Code Style** | **10** |  |
| **Readme** | **25** |  |
| **Total** | **100** |  |

**Required Functionality**

Get a single channel of the oscilliscpe to display with reliable triggering that holds the waveform at a single point on the left edge of the display. A 220Hz waveform should display something similar to that shown in the screen shot at the top of this page.

* USe a package file to contain all your component declarations.
* Use seperate datapath and control unit.
* Your datapath must use processes which are similar to our basic building block (counter, register, mux, etc.). I do not want to see one massive process that attempts to do all the work in the datapath.
* Testbench for the flagRegister.
* Testbench for the control unit.

**B-level functionality**

Meet all the requirements of required functionality. Add a second channel (in green). Integrate the button debouncing strategy in HW #7 to debounce the buttons controlling the trigger time and trigger volage. Move the cursors on the screen.

**A-level functionality**

Meet all the requirements of B-level functionality. Use the trigger voltage marker to establish the actual trigger voltage used to capture the waveform. As the trigger is moved up and down you should see the point at which the waveform intersects the left side of the screen change

**Lab notebook**

* **Introduction** - Provide a brief overview of the problem.
* **Implementation** - Provide block-diagram of your solution using the signal names in your code. The block diagram given above is somewhat incomplete, make sure to include corrections to this diagram. For each module that you built, explain its overall purpose, inputs, outputs, and behavior. Include all your vhdl files (code and testbench), wcfg file, and bit files. Put these in a folder called "code".
* **Test/Debug** - Briefly describe the methods used to verify system functionality. List the major problems you encountered and how you fixed them. This should cover all the problems you encountered in the lab and how you fixed them. Break each problem and solution into separate paragraphs.
* **Capability** - Well you have built a oscilloscope, what are its capabilities?

1. The horizontal axis represents time. There are 10 major divisions on the display; how long does each major division represent?
2. Each major time division is split into 4 minor division, how long does each minor division represent?
3. Generate a sine wave that can be fully captured on your display (like the yellow channel in the image at the top of this web page). record its height in major and minor vertical divisions. Measure this same audio output using the break out audio cable. Record the peak-to-peak voltage. Compute the number of volts in each major and minor vertical division.
4. Starting at address 0, how long does it take to fill the entire memory with audio samples (coming in at 48kHz)?
5. How long does it take to completely draw the display once?
6. The question is likely relevant to Lab 3 - how long does the vsynch signal go high at the end during the Front Porch, Synch, and Back Porch?

* **Conclusion** - Explain what your learned from this lab and what changes you would recommend in future years to this lab or the lectures leading up to this lab.